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Hai Jiang; Shixin Cheng; Yongming He; Bo Sun;
Wireless Communications and Networking Conference, 2002. WCNC2002. 2002
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SoutheastCon, 2002. Proceedings IEEE , 5-7 April 2002
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[Abstract] [PDF Full-Text (391 KB)] **IEEE CNF**

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28 **A simple yet effective technique for partitioning**
Hyunchul Shin; Chunghee Kim;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume:
Issue: 3 , Sept. 1993
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29 **A 600-MHz 54×54-bit multiplier with rectangular-styled Wallace tre**
Itoh, N.; Naemura, Y.; Makino, H.; Nakase, Y.; Yoshihara, T.; Horiba, Y.;
Solid-State Circuits, IEEE Journal of , Volume: 36 Issue: 2 , Feb. 2001

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1 VLSI circuit partitioning by cluster-removal using iterative improvement techniques 88%

Shantanu Dutt , Wenyong Deng

Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997

Move-based iterative improvement partitioning methods such as the Fiduccia-Mattheyses (FM) algorithm and Krishnamurthy's Look-Ahead (LA) algorithm are widely used in VLSI CAD applications largely due to their time efficiency and ease of implementation. This class of algorithms is of the "local improvement" type. They generate relatively high quality results for small and medium size circuits. However, as VLSI circuits become larger, these algorithms are not so effective on them as direct partiti ...

2 Parametric query optimization 88%

Yannis E. Ioannidis , Raymond T. Ng , Kyuseok Shim , Timos K. Sellis

The VLDB Journal — The International Journal on Very Large Data Bases May 1997

Volume 6 Issue 2

In most database systems, the values of many important run-time parameters of the system, the data, or the query are unknown at query optimization time. Parametric query optimization attempts to identify at compile time several execution plans, each one of which is optimal for a subset of all possible values of the run-time parameters. The goal is that at run time, when the actual parameter values are known, the appropriate plan should be identifiable with essentially no overhead. We present a g ...

3 Register allocation across procedure and module boundaries 82%

Vatsa Santhanam , Daryl Odnert

ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1990 conference on Programming language design and implementation June 1990

Volume 25 Issue 6

This paper describes a method for compiling programs using interprocedural register allocation. A strategy for handling programs built from multiple modules is presented, as well as algorithms for global variable promotion and register spill code motion. These algorithms attempt to address some of the shortcomings of previous interprocedural register allocation strategies. Results are given for an implementation on a single register file RISC-based architec ...

4 Synthesis and floorplanning for large hierarchical FPGAs 82%

H. Krupnova , C. Rabedaoro , G. Saucier

Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays February 1997

5 Session 4A: placement I: Mongrel: hybrid techniques for standard cell placement 80%

Sung Woo Hur , John Lillis

Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design November 2000

We give an overview of a standard-cell placer *Mongrel.* The prototype tool adopts a *middle-down* methodology in which a grid is imposed over the layout area and cells are assigned to bins forming a *global placement.* The optimization technique applied in this phase is based on the *Relaxation-Based Local Search* (RBLS) framework in which a combinatorial search mechanism is driven by an analytical engine. This enables a more global view of the problem and results in complex ...

6 A logic partitioning procedure by interchanging clusters 80%

Tadakatsu Ishiga , Tokinori Kozawa , Shoji Sato

Proceedings of the 12th design automation conference January 1975

A logic partitioning procedure for computer aided design of LSI's which gets solutions by interchanging clusters is described. The procedure of generating clusters has some distinct features which assure that the clusters are suitable as units for interchanging. The cluster concept gives the Kernighan and Lin algorithm foresight and efficiency, and because of these, iteration of interchanging leads to a good solution. Results of partition for a variety of LSI's obtained with the ...

7 A general purpose multiple way partitioning algorithm 80%

Ching-Wei Yeh , Chung-Kuan Cheng , Ting-Ting Y. Lin

Proceedings of the 28th conference on ACM/IEEE design automation conference June 1991

8 A linear-time heuristic for improving network partitions 77%

C. M. Fiduccia , R. M. Mattheyses

Proceedings of the nineteenth design automation conference January 1982

An iterative mincut heuristic for partitioning networks is presented whose worst case computation time, per pass, grows linearly with the size of the network. In practice, only a very small number of passes are typically needed, leading to a fast approximation algorithm for mincut partitioning. To deal with cells of various sizes, the algorithm progresses by moving one cell at a time between the blocks of the partition while maintaining a desired balance based on the size of the blocks rath ...

9 Algorithms for data migration with cloning 77%

Samir Khuller , Yoo-Ah Kim , Yung-Chun (Justin) Wan

Proceedings of the twenty-second ACM SIGMOD-SIGACT-SIGART symposium on Principles of database systems June 2003

Our work is motivated by the problem of managing data on storage devices, typically a set of disks. Such high demand storage servers are used as web servers, or multimedia servers for handling high demand for data. As the system is running, it needs to dynamically respond to changes in demand for different data items. In this work we study the *data migration problem*, which arises when we need to quickly change one storage configuration into another. We show that this problem is NP-hard. I ...

10 A linear-time heuristic for improving network partitions 77%

C. M. Fiduccia , R. M. Mattheyses

Papers on Twenty-five years of electronic design automation June 1988

11 Device-level design: Automatic transistor and physical design of FPGA tiles from an architectural specification 77%

Ketan Padalia , Ryan Fung , Mark Bourgeault , Aaron Egier , Jonathan Rose

Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays February 2003

One of the most difficult and time-consuming steps in the creation of an FPGA is its transistor-level design and physical layout. Modern commercial FPGAs typically consume anywhere from 50 to 200 man-years simply in the layout step. To date, automated tools have only been employed in small parts of the periphery and programming circuitry. The core tiles, which are repeated many times, are subject to painstaking manual design and layout. In this paper we present a new system (called GILES, for Go ...

12 Cluster assignment for high-performance embedded VLIW processors 77%

Viktor S. Lapinskii , Margarida F. Jacome , Gustavo A. De Veciana

ACM Transactions on Design Automation of Electronic Systems (TODAES) July 2002

Volume 7 Issue 3

Clustering is an effective method to increase the available parallelism in VLIW datapaths without incurring severe penalties associated with a large number of register file ports. Efficient utilization of a clustered datapath requires careful binding/assignment of operations to clusters. The article proposes a binding algorithm that effectively explores trade-offs between in-cluster operation serialization and delays associated with data transfers between clusters. Extensive experimental evidenc ...

13 New faster Kernighan-Lin-type graph-partitioning algorithms 77%

Shantanu Dutt

Proceedings of the IEEE/ACM international conference on Computer-aided design November 1993

14 A combined hierarchical placement algorithm 77%

Hyunchul Shin , Chunghee Kim , Wonjong Kim , Myoungsub Oh , Kwangjoon Rhee , Seogyun Choi , Heasoo Chung

Proceedings of the IEEE/ACM international conference on Computer-aided design November 1993

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